

FDD8870_F085 / FDU8870_F085

N-Channel PowerTrench® MOSFET 30V, 160A, 3.9mΩ

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(ON)}$ and fast switching speed.

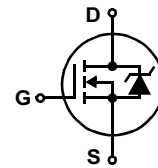
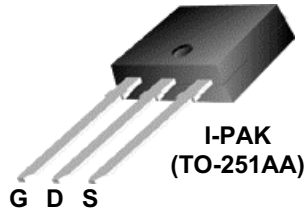
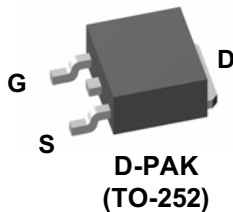
Applications

- DC/DC converters



Features

- $r_{DS(ON)} = 3.9m\Omega$, $V_{GS} = 10V$, $I_D = 35A$
- $r_{DS(ON)} = 4.4m\Omega$, $V_{GS} = 4.5V$, $I_D = 35A$
- High performance trench technology for extremely low $r_{DS(ON)}$
- Low gate charge
- High power and current handling capability
- Qualified to AEC Q101
- RoHS Compliant



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current		
	Continuous ($T_C = 25^\circ C$, $V_{GS} = 10V$) (Note 1)	160	A
	Continuous ($T_C = 25^\circ C$, $V_{GS} = 4.5V$) (Note 1)	150	A
	Continuous ($T_{amb} = 25^\circ C$, $V_{GS} = 10V$, with $R_{\theta JA} = 52^\circ C/W$)	21	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	690	mJ
P_D	Power dissipation	160	W
	Derate above $25^\circ C$	1.07	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	$^\circ C$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-252, TO-251	0.94	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, TO-251	100	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in ² copper pad area	52	$^\circ C/W$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8870	FDD8870_F085	TO-252AA	13"	12mm	2500 units
FDU8870	FDU8870_F085	TO-251AA	Tube	N/A	75 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.2	-	2.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 35\text{A}, V_{GS} = 10\text{V}$	-	0.0032	0.0039	Ω
		$I_D = 35\text{A}, V_{GS} = 4.5\text{V}$	-	0.0036	0.0044	
		$I_D = 35\text{A}, V_{GS} = 10\text{V}, T_J = 175^\circ\text{C}$	-	0.0051	0.0063	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	5160	-	pF
C_{OSS}	Output Capacitance		-	990	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	590	-	pF
R_G	Gate Resistance	$V_{GS} = 0.5\text{V}, f = 1\text{MHz}$	-	2.1	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V to } 10\text{V}$	-	91	118	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0\text{V to } 5\text{V}$	-	48	62	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V to } 1\text{V}$	-	5	6.5	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 15\text{V}$ $I_D = 35\text{A}$ $I_g = 1.0\text{mA}$	-	14	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	9	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	18	-	nC

Switching Characteristics ($V_{GS} = 10\text{V}$)

t_{ON}	Turn-On Time	$V_{DD} = 15\text{V}, I_D = 35\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 3.3\Omega$	-	-	139	ns
$t_{d(ON)}$	Turn-On Delay Time		-	9	-	ns
t_r	Rise Time		-	83	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	83	-	ns
t_f	Fall Time		-	42	-	ns
t_{OFF}	Turn-Off Time		-	-	189	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 35\text{A}$	-	-	1.25	V
		$I_{SD} = 15\text{A}$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 35\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	37	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 35\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	21	nC

Notes:

- Package current limitation is 35A.
- Starting $T_J = 25^\circ\text{C}, L = 1.77\text{mH}, I_{AS} = 28\text{A}, V_{DD} = 27\text{V}, V_{GS} = 10\text{V}$.

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

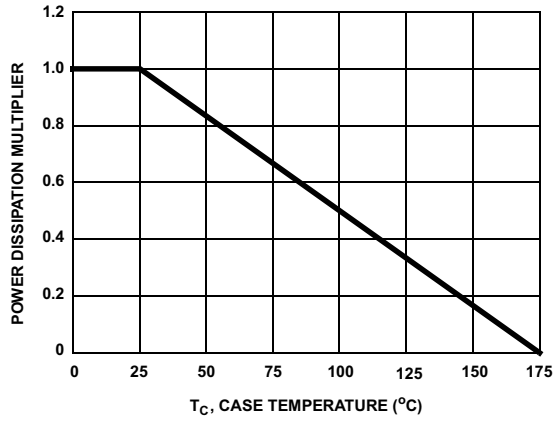


Figure 1. Normalized Power Dissipation vs Case Temperature

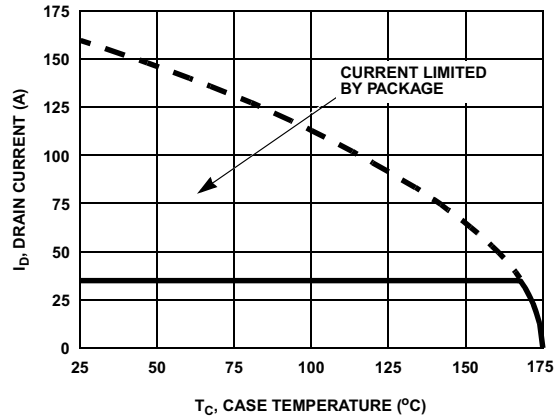


Figure 2. Maximum Continuous Drain Current vs Case Temperature

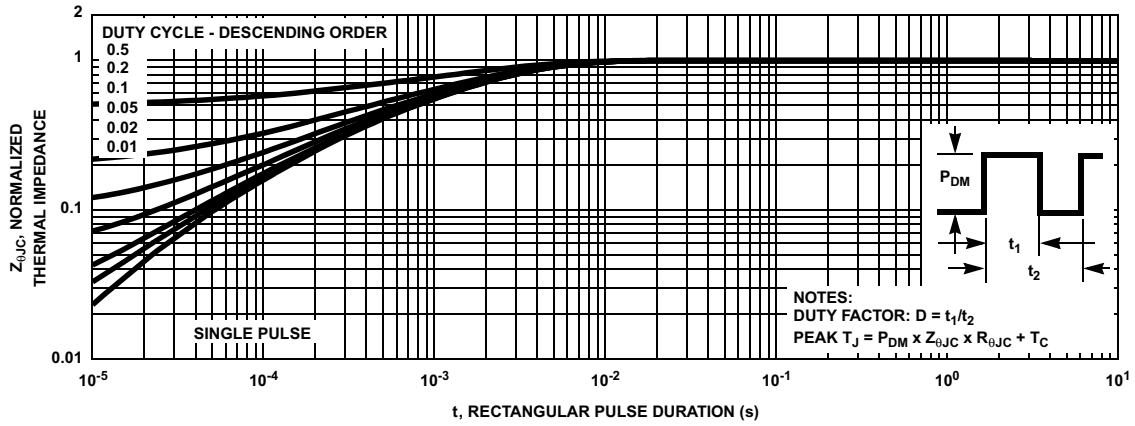


Figure 3. Normalized Maximum Transient Thermal Impedance

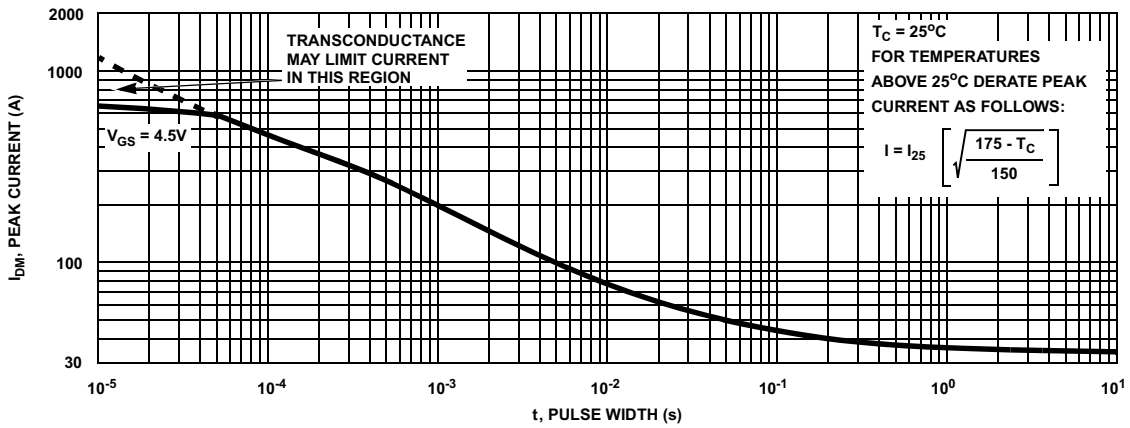


Figure 4. Peak Current Capability

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

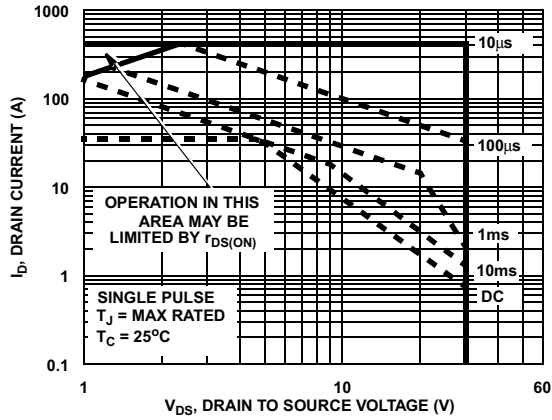
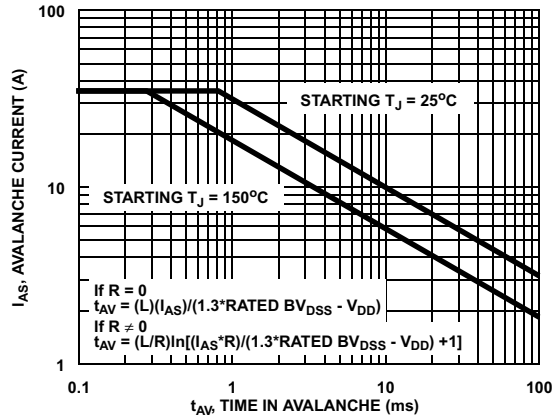


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515
Figure 6. Unclamped Inductive Switching Capability

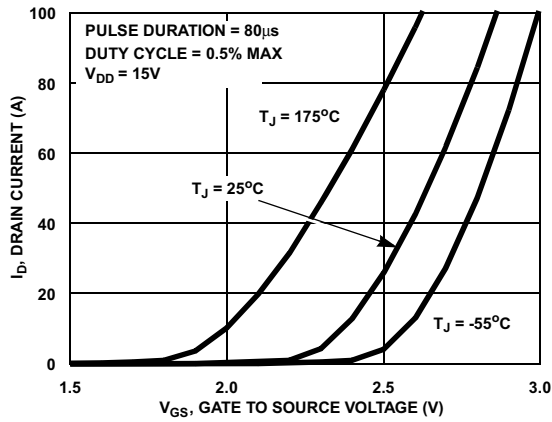


Figure 7. Transfer Characteristics

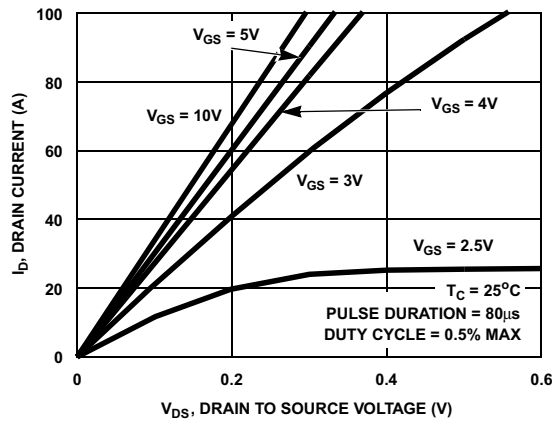


Figure 8. Saturation Characteristics

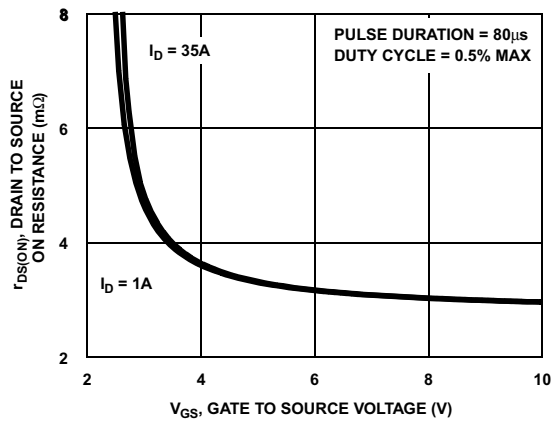


Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current

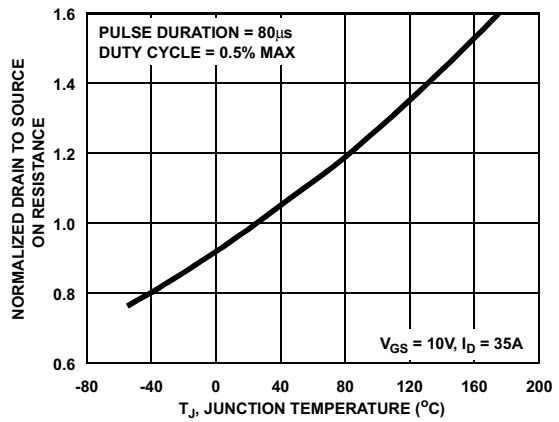


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

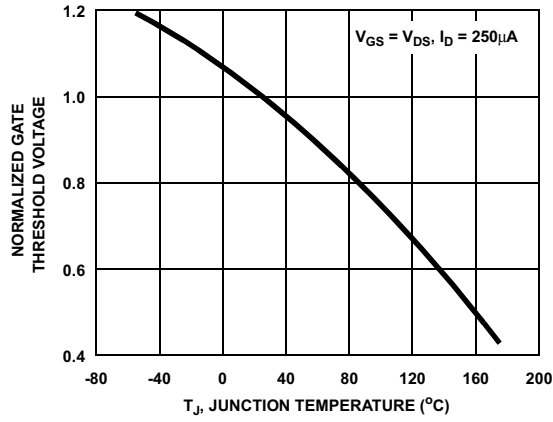


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

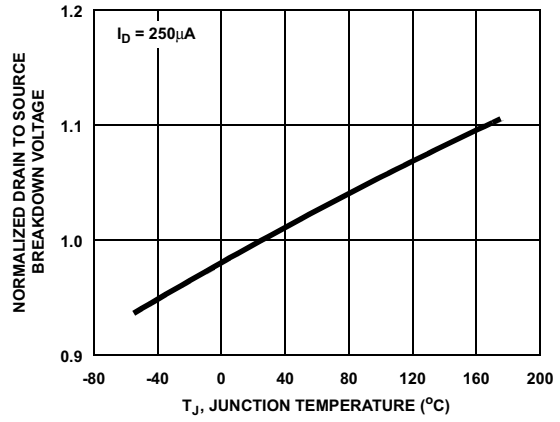


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

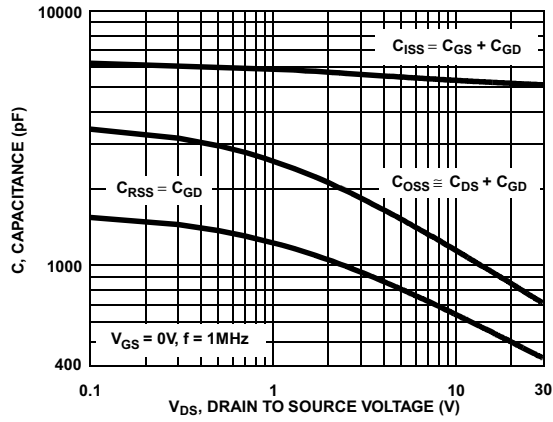


Figure 13. Capacitance vs Drain to Source Voltage

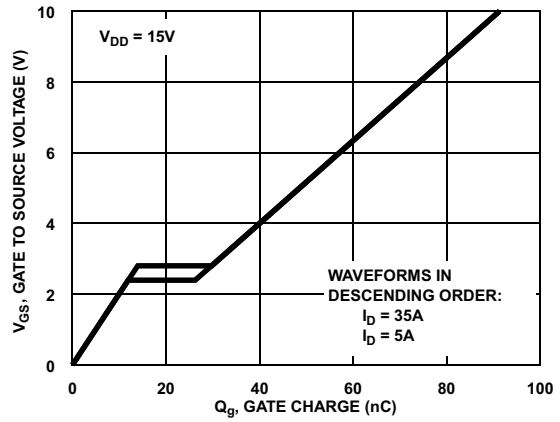


Figure 14. Gate Charge Waveforms for Constant Gate Current

Test Circuits and Waveforms

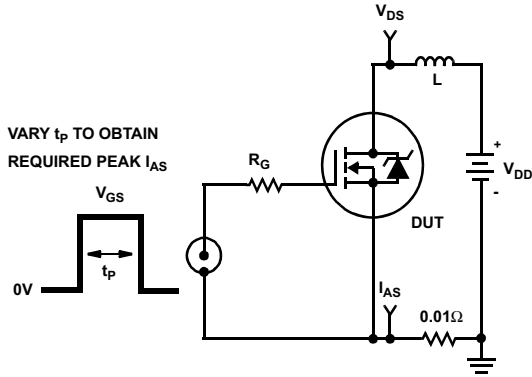


Figure 15. Unclamped Energy Test Circuit

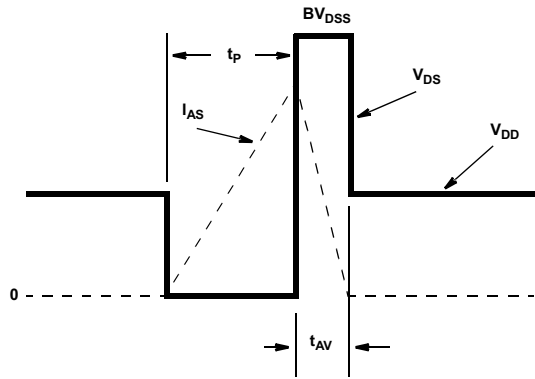


Figure 16. Unclamped Energy Waveforms

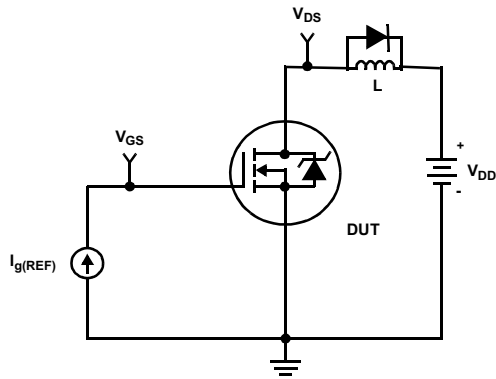


Figure 17. Gate Charge Test Circuit

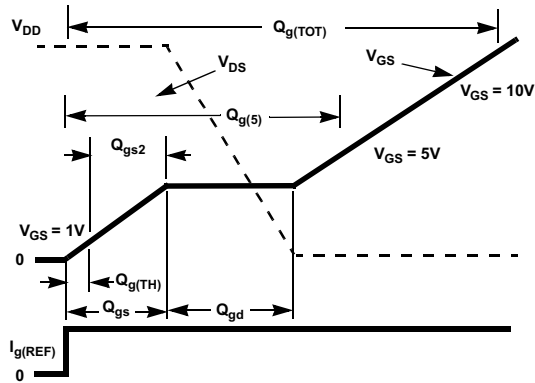


Figure 18. Gate Charge Waveforms

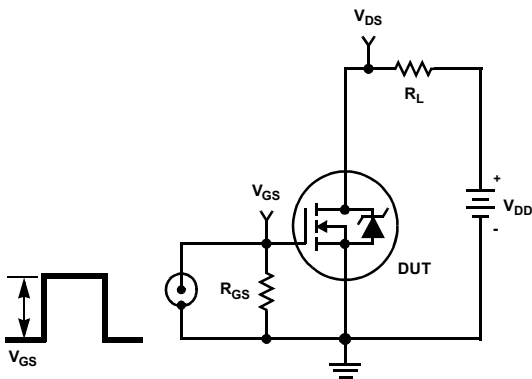


Figure 19. Switching Time Test Circuit

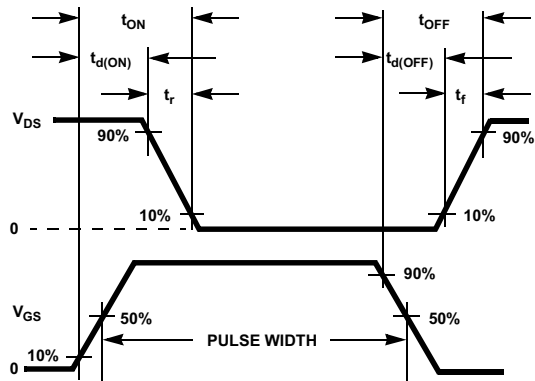


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A ($^{\circ}C$), and thermal resistance $R_{\theta JA}$ ($^{\circ}C/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (\text{EQ. 1})$$

In using surface mount devices such as the TO-252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + Area)} \quad (\text{EQ. 2})$$

Area in Inches Squared

$$R_{\theta JA} = 33.32 + \frac{154}{(1.73 + Area)} \quad (\text{EQ. 3})$$

Area in Centimeters Squared

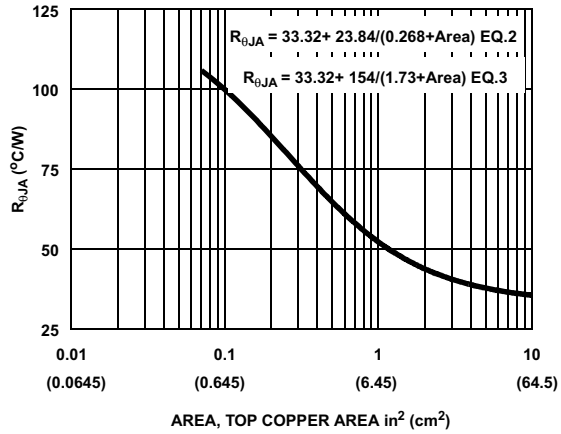


Figure 21. Thermal Resistance vs Mounting Pad Area

SABER Electrical Model

```

rev July 2003
template FDD8870 n2,n1,n3 =m_temp
electrical n2,n1,n3
number m_temp=25
{
var i iscl
dp..model dbodymod = (isl=1.3e-11,ikf=10,nl=1.01,rs=1.8e-3,trs1=8e-4,trs2=2e-7,cjo=2e-9,m=0.57,tt=1e-10,xti=0.9)
dp..model dbreakmod = (rs=8e-2,trs1=1e-3,trs2=-8.9e-6)
dp..model dplcapmod = (cjo=1.6e-9,isl=10e-30,nl=10,m=0.38)
m..model mmedmod = (type=_n,vto=1.76,kp=10,is=1e-30,tox=1)
m..model mstrongmod = (type=_n,vto=2.2,kp=650,is=1e-30,tox=1)
m..model mweakmod = (type=_n,vto=1.47,kp=0.05,is=1e-30,tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-3)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-3,voff=-4)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-2,voff=-0.5)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=-0.5,voff=-2)
c.ca n12 n8 = 4.2e-9
c.cb n15 n14 = 4.2e-9
c.cin n6 n8 = 4.7e-9

```

```

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

```

```

spe.ebreak n11 n7 n17 n18 = 32.7
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

```

```
i.it n8 n17 = 1
```

```

l.lgate n1 n9 = 5e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 2e-9

```

```

res.rlgate n1 n9 = 50
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 20

```

```

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u, temp=m_temp
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u, temp=m_temp
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u, temp=m_temp

```

```

res.rbreak n17 n18 = 1, tc1=8.3e-4,tc2=-4e-7
res.rdrain n50 n16 = 1.57e-3, tc1=2e-4,tc2=8e-6
res.rgate n9 n20 = 2.1
res.rslc1 n5 n51 = 1e-6, tc1=9e-4,tc2=1e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 1.2e-3, tc1=8e-3,tc2=1e-6
res.rvthres n22 n8 = 1, tc1=-2e-3,tc2=-9.5e-6
res.rvtemp n18 n19 = 1, tc1=-2.6e-3,tc2=2e-7
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

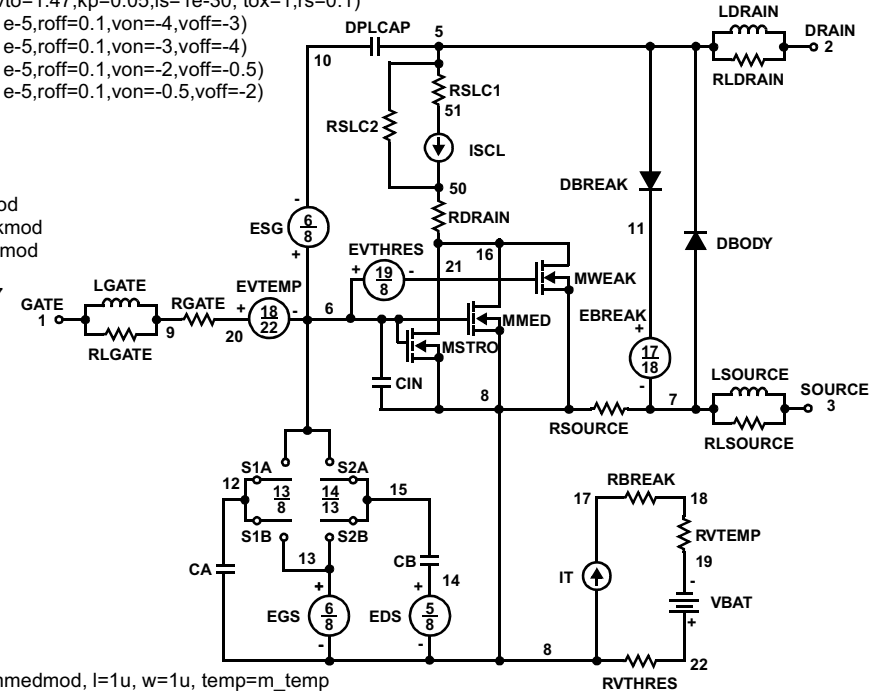
```

```
v.vbat n22 n19 = dc=1
```

```

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/500))** 10)
}
}

```



FDD8870_F085/FDU8870_F085 N-Channel PowerTrench® MOSFET

PSPICE Thermal Model

REV 23 July 2003

FDD8870T

CTHERM1 TH 6 1e-3
CTHERM2 6 5 2e-3
CTHERM3 5 4 3e-3
CTHERM4 4 3 9e-3
CTHERM5 3 2 1e-2
CTHERM6 2 TL 2e-2

RTHERM1 TH 6 3e-2
RTHERM2 6 5 8e-2
RTHERM3 5 4 1.1e-1
RTHERM4 4 3 1.6e-1
RTHERM5 3 2 1.72e-1
RTHERM6 2 TL 2e-1

SABER Thermal Model

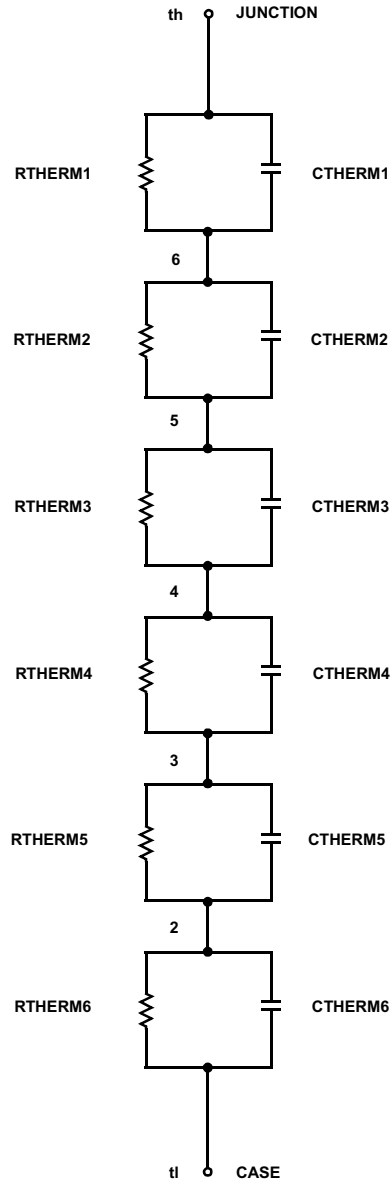
SABER thermal model FDD8870T

template thermal_model th tl

thermal_c th, tl

```
{  
  ctherm.ctherm1 th 6 =1e-3  
  ctherm.ctherm2 6 5 =2e-3  
  ctherm.ctherm3 5 4 =3e-3  
  ctherm.ctherm4 4 3 =9e-3  
  ctherm.ctherm5 3 2 =1e-2  
  ctherm.ctherm6 2 tl =2e-2
```

```
rtherm.rtherm1 th 6 =3e-2  
rtherm.rtherm2 6 5 =8e-2  
rtherm.rtherm3 5 4 =1.1e-1  
rtherm.rtherm4 4 3 =1.6e-1  
rtherm.rtherm5 3 2 =1.72e-1  
rtherm.rtherm6 2 tl =2e-1  
}
```



FDD8870_F085/FDU8870_F085 N-Channel PowerTrench[®] MOSFET



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| AX-CAP™* | Global Power Resource™ | Programmable Active Droop™ | franchise |
| BitSiC® | Green Bridge™ | QFET® | TinyBoost™ |
| Build it Now™ | Green FPS™ | QS™ | TinyBuck™ |
| CorePLUS™ | Green FPS™ e-Series™ | Quiet Series™ | TinyCalc™ |
| CorePOWER™ | Gmax™ | RapidConfigure™ | TinyLogic® |
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| Current Transfer Logic™ | ISOPLANAR™ | Saving our world, 1mW/W/kW at a time™ | TinyPWM™ |
| DEUXPEED® | Marking Small Speakers Sound Louder and Better™ | SignalWise™ | TinyWire™ |
| Dual Cool™ | MegaBuck™ | SmartMax™ | TranSiC® |
| EcoSPARK® | MICROCOUPLER™ | SMART START™ | TriFault Detect™ |
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ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.Fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.